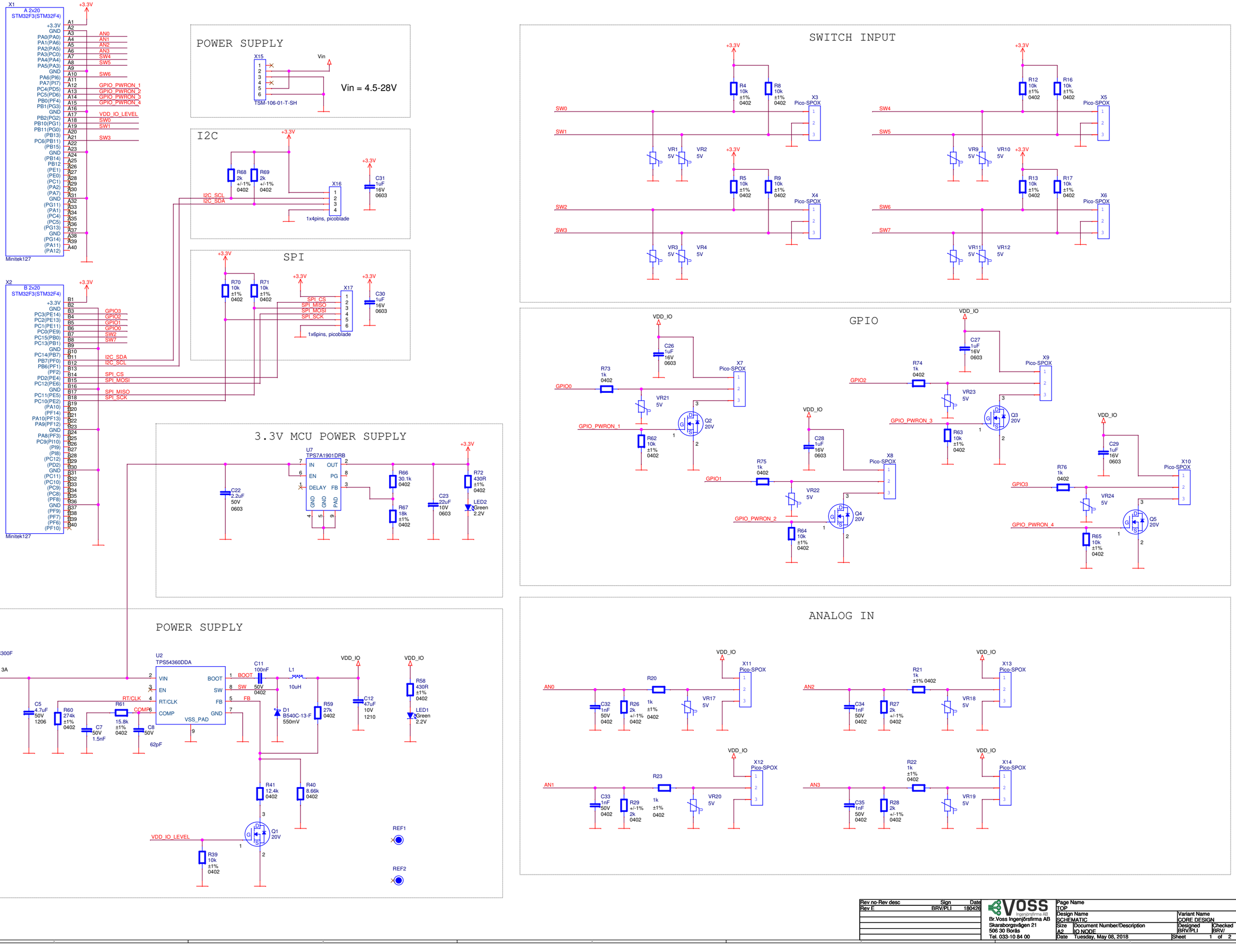

Rev no-Rev desc	Sign	Date
Rev E	BRV/PLI	180426

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REV A:
- Initital design generation 1

REV B:
- New board outline

REV C:
- Initital design generation 2
- New connectors for power and IO. Smaller footprint

REV D:
- Moved SW3 to PC15
- Connectd missing signal GPIO4 in CPU connector
- /SPI_CS connected to PD2

REV E:
- Added serie resistors on GPIO to protect CPU When VDD_IO is 5V
- New 6 pin power connector

Rev no-Rev desc	Sign	Date
P001-Initial Design	BRV/XX	170823

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